

FACSIMILE TRANSMISSION

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Date: March 5, 2003

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Application of

Applicants : Chandra V. Mouli and Ceredig Roberts

Serial No. : 09/648,044

Filed : August 25, 2000

Confirm No. : 6800

Title : **METHOD AND DEVICE TO REDUCE GATE-INDUCED DRAIN
LEAKAGE (GIDL) CURRENT IN THIN GATE OXIDE MOSFETs**

Docket No. : MIO 0054 PA

Examiner : O. Nadav

Art Unit : 2811



Patents, Trademarks and Related Matters

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Response Under 37 CFR 1.116

Expedited Procedure

Examining Gr up 2811

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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William A. Jviden

42,695
Reg. No.

Sir:

AMENDMENT AFTER FINAL REJECTION

This paper is being filed in response to the office action made final and dated February 24, 2003 in the identified application. Reconsideration and reexamination are respectfully requested in light of the amendments and remarks below.

In the Claims

Please note that the entire set of presently pending claims has been reproduced below for the convenience of the Examiner. Amended claims are indicated as such in the parenthetical following each claim number.

1. (Currently Amended) A circuit structure comprising:

a semiconductor layer;

an oxide layer formed on said semiconductor layer;

a gate structure formed on said oxide layer having first and second leading edges; and